Selektie materiaalkunde

WH89-PAL

PARALLEL INTERFACE FOR THE

WH/Z89 COMMPUTER

Implementatie 20 feb 83

basis poort 320 Q = DØ = 208_{10}

data kanaal A	DØ (208_{10})	→
data kanaal C	D2	→
data kanaal B	D1	→
kontrole poort	D3	

(backside H89)

D-kormekter - female 25 pe

pin 1 ... 8	DØ ... D7
pin 9 ... 16	DØ ... D7
pin 17 - 24	DØ ... D7
pin 25 is massa	

INDEX

WH89-PAL

INTRODUCTION...

The WH89-PAL is a general purpose programmable parallel I/O device designed to be compatable with any peripheral that requires data to be transfered in the 8 bit parallel format.

The WH89-PAL uses the INTEL (r) 8255A 3 port programmable parallel interface and is completely compatable with the 8080, 8080A, Z80, and Z80A microprocessors such as what are currently being used by HEATH / ZENITH Corp.

With the WH89-PAL the programmer has the capability to use the WH/Z89 computer with parallel printers such as the CENTRONICS (r) or to even operate many types of parallel interface style A/D, D/A converters.

INSTALLATION...

The complete board installs in either one of the two inside buss connections found on the right hand side of the CPU card inside the WH/Z89 computer. It is installed with the deep notch and the fuse on the top.

Before installing the WH89-PAL be sure that you have jumpered the circuit board for the port address that you wish to use in the system. The port programming is done by the placement of a jumper from location 'E' on the circuit board to another lettered jumper location... 'A','B','C', or 'D'.

The I/O map is as follows and the programming of parallel interface will be discussed in detail further on in this manual.

Jumpers from -- to =

A	E	= PORT 320 Q
B	E	= PORT 330 Q
C	E	= PORT 340 Q
D	E	= PORT 370 Q

kan niet want cassette poort is alleen gedecodeerd voor 371 en 370

You may place a jumper at any ONE of these locations.

Door meeste I/O PROM (444-61) wordt dit 170 - 177

CIRCUIT DISTCRIPTION...

The layout and design is simplicity in itself, the 8255A is almost a completely self contained interface device and needs very little support.

Data is transfered via a bidirectional buss through a tristate bidirectional buffer IC2, at that point data is latchcd into IC1. The only logic required to operate the complete board is the (RD), (WR), and (CS) pulses.

The (RD) pulse (read enable) is inverted via IC3 to enable IC2 but is connected directly through to pin 5 of IC1. A low at pin 6 of J2 will enable the parallel interface to put data directly on the buss through the buffer (IC2) and J1.

The (WR) pulse (write enable) is inverted by IC3 also and used to enable buffer IC2. The uninverted (WR) pulse is connected directly to pin 36 of IC1. A low at pin 7 of J2 will cause data on the buss to be 'dumped' into the parallel interface.

The (CS) pulse (chip select) is placed directly on pin 19 of IC2 and pin 6 of IC1. This pulse is used to 'decide' two basic operations....

1.) When this pulse goes low and (RD) or (WR) goes low at the same time the WH89-PAL is selected to output or input a byte of eight bit code.

2.) Depending where you have placed the port program jumper the (CS) pulse will come via pins 9, 10, 11, or 12 of J2.

The output connectors J3, J4 and J5 are the three I/O ports that communicate with the outside world through the 8255A. Pins 1 and 10 of each of these ports has a five volt supply available with pin 1 being the ground and pin 10 being the positive five volts. This five volt supply is fused through a .2 anp fuse, F1. This gives the systems designer an easier way to aquire a bias voltage, which is required at times with different types of A/D and D/A converters.

C1 and C2 are used to decouple any high and low speed spikes or pulses that could possibly disrupt the operation of the 8255A.

PROGRAMMING...

The programming of the WH89-PAL is easy and very quick

to do. The only time that may be required is trying to decide which is the best method for you, as there are three modes of operation and over twenty five differant software I/O configurations.

It is beyond the scope of this manual to show and discuss all of these methodes at this time. It is suggested that the programmer acquire an 8255A INTEL (r) programmers guide from the local INTEL (r) distributor in your area. Most distributors will be more than happy to send you a copy of this 20 page booklet for a very small charge.

A test program is included here along with a model program written in 8080 assembly code. The test program is very easily punched into the WH/Z89 via the 'SUB' command of the monitor program.

TEST PROGRAM.....

This program will output to port A of the WH89-PAL a 'HI' then 'LOW' on all data bits (D0-D7).

Start the test program, using the 'SUB' operation at memory location 042200Q.

```
076
200
323
23
076
377        All bits set high
323
320        Output to port 320Q port 'A', this can be changed to
           port 'B', etc by changing this to 321Q in which case
041        the code will go out port 320Q channel 'B'
377
070
```

053
175
264
302
213
042
[illegible]
000 This is the new code to bring D0-D7 'low'
323
320
041
377
070
053
075
264
302
230
042
303 Jump back and do this again (mem. location 042204Q)
204
042

End of the test program.

The following is a model of how code is transfered out to the WH89-PAL from an assembly language level.

Please note, all high level language programmers there is a device driver for you also written under HDOS and CPM (r) the device driver for HDOS is called 'PA.DVD', the device driver for CPM is a modified version of the 'USER.ASM' program. Both of these are available from your local Heath/Zenith operation or from T.U.G.S. in West Germany.

MODEL OF AN OUTPUT ONLY ROUTINE...

```
            .
            .
            .
            .
PALDVD      MVI   A,200Q        THIS SETS THE 8255A FOR AN OUTPUT
                                 ON ALL CHANNELS A, B, C.
            OUT   323Q          IN ALL CASES THIS MODE WORD GOES
                                 TO CHANNEL 'C' TO SET UP THE
                                 OPERATION.
            LXI   H,BUFFER      LOAD IN THE FIRST ADDRESS OF THE
                                 BUFFER.
OUTPUT      LDA   M             MOVE CONTENTS OF H,L TO 'A' REG.
            OUT   320Q          OUT TO PORT 'A' OF 8255A
            .
            .
            .
            .
```

EAMPLE OF AN OUTPUT ON PORT 'A' WITH INPUT ON PORT 'B'

```
            .
            .
```

```
PALDVD   MVI  A,202Q        MODE '0' CONTROL '2'
         OUT  323Q          OUT TO CONTROL PORT
         LXI  H,BUFFER      LOAD IN THE FIRST BUFFER ADD.
         .
         .
         .
OUTPUT   LDA  M             MOVE CONTENTS OF H,L TO 'A' REG.
         OUT  320Q          OUT PORT 320Q CHANNEL A
         RET                RETURN
INPUT    IN   321Q          IN PORT 320 CHANNEL B
         MOV  B,A           MOVE THE CONTENTS OF REG 'A' TO
                            REG 'B' (EXAMPLE)
         RET                RETURN
```

DEL OF A BIDIRECTIONAL ROUTINE WITH CHANNEL 'C' AS THE HANDSHAKE LINE, AND CHANNEL 'A' AS THE BIDIRECTIONAL LINE

```
PALDVD   MVI  A,301Q        CONTROL WORD
         OUT  323Q          CONTROL WORD OUT TO CHANNEL 'C'
         CALL HANDSHK       SEE IF THE DEVICE IS READY
         LXI  H,BUFFER      INPUT BUFFER
         LDA  M             LOAD 'A' REG DIRECT FROM MEM. LOC.
         OUT  320Q          OUTPUT TO CHANNEL 'A'
```

```
        IN    320Q          INPUT FROM CHANEL 'A'

        MOV   B,A           MOVE INPUT BYTE TO 'B' REG.
                            ETC,ETC (EXAMPLE)
        .
        .
        .
        .
HANDSHK IN    323Q          INPUT THE HANDSHAKE BIT
        ANI   01000000B     SEE IF THE 'ACK' LINE IS HIGH
        JNZ   HANDSHK       KEEP LOOKING UNTILL IT GOES LOW
        RET                 RETURN

                    EOF
```

8255A

SPECIFICATIONS

AND

PROGRAMMING

8255A OPERATIONAL DESCRIPTION

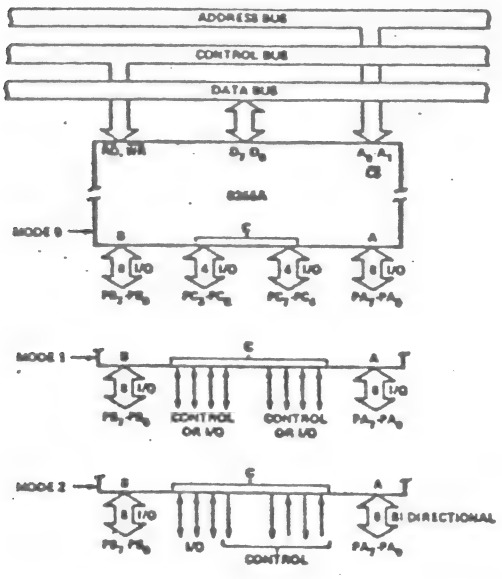
Mode Selection

There are three basic modes of operation that can be selected by the system software:

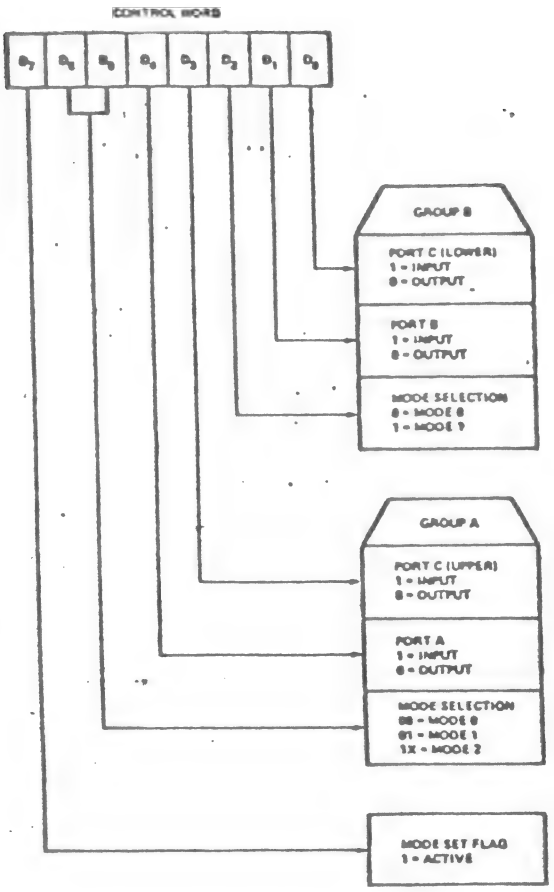
Mode 0 – Basic Input/Output
Mode 1 – Strobed Input/Output
Mode 2 – Bi-Directional Bus

When the reset input goes "high" all ports will be set to the input mode (i.e., all 24 lines will be in the high impedance state). After the reset is removed the 8255A can remain in the input mode with no additional initialization required. During the execution of the system program any of the other modes may be selected using a single output instruction. This allows a single 8255A to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance; Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.



Basic Mode Definitions and Bus Interface

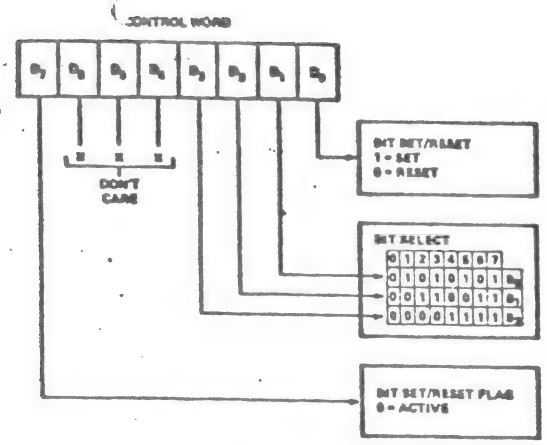


Mode Definition Format

The mode definitions and possible mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 8255A has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUTput instruction. This feature reduces software requirements in Control-based applications.



Bit Set/Reset Format

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

Interrupt Control Functions

When the 8255A is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the Programmer to disallow or allow a specific I/O device to interrupt the CPU without affecting any other device in the interrupt structure.

INTE flip-flop definition:

(BIT-SET) — INTE is SET — Interrupt enable
(BIT-RESET) — INTE is RESET — Interrupt disable

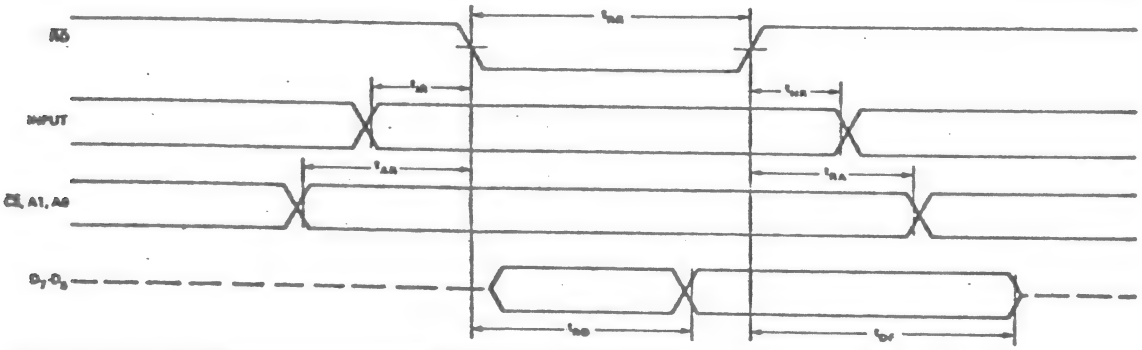
Note: All Mask flip-flops are automatically reset during mode selection and device Reset.

Operating Modes

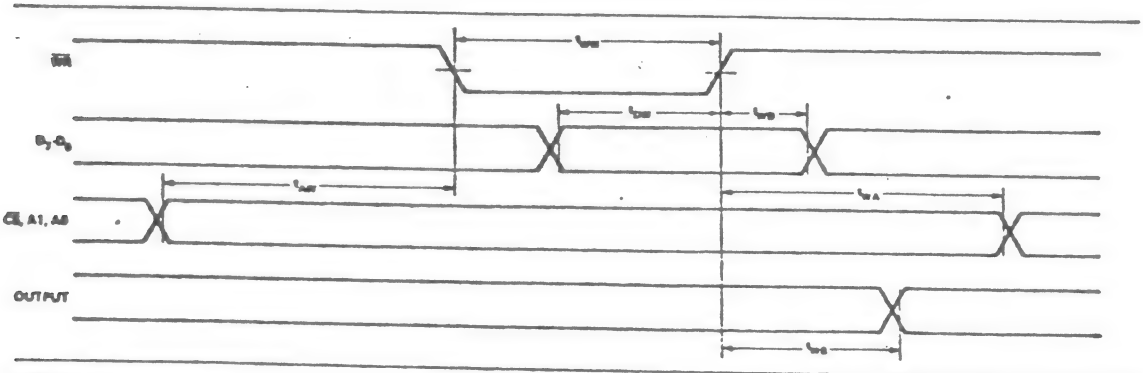
MODE 0 (Basic Input/Output). This functional configuration provides simple input and output operations for each of the three ports. No "handshaking" is required, data is simply written to or read from a specified port.

Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports.
- Any port can be input or output.
- Outputs are latched.
- Inputs are not latched.
- 16 different Input/Output configurations are possible in this Mode.



MODE 0 (Basic Input)

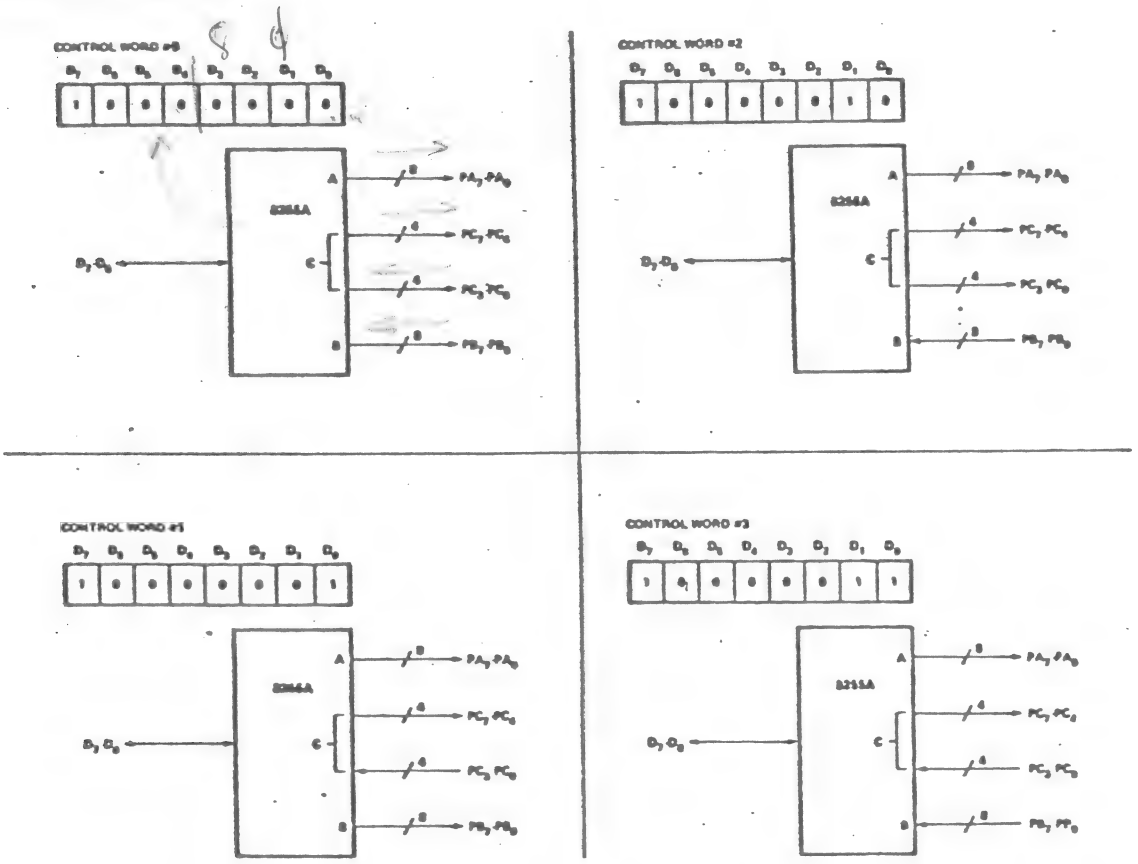


MODE 0 (Basic Output)

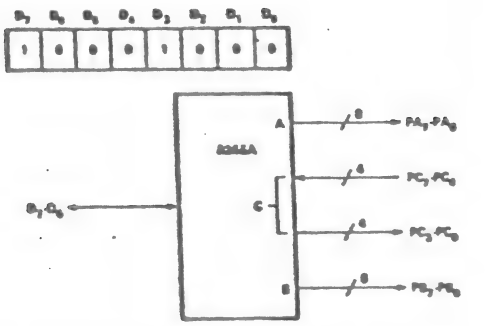
MODE 0 Port Definition

A		B		GROUP A			GROUP B	
D_6	D_5	D_1	D_0	PORT A	PORT C (UPPER)	#	PORT B	PORT C (LOWER)
0	0	0	0	OUTPUT	OUTPUT	0	OUTPUT	OUTPUT
0	0	0	1	OUTPUT	OUTPUT	1	OUTPUT	INPUT
0	0	1	0	OUTPUT	OUTPUT	2	INPUT	OUTPUT
0	0	1	1	OUTPUT	OUTPUT	3	INPUT	INPUT
0	1	0	0	OUTPUT	INPUT	4	OUTPUT	OUTPUT
0	1	0	1	OUTPUT	INPUT	5	OUTPUT	INPUT
0	1	1	0	OUTPUT	INPUT	6	INPUT	OUTPUT
0	1	1	1	OUTPUT	INPUT	7	INPUT	INPUT
1	0	0	0	INPUT	OUTPUT	8	OUTPUT	OUTPUT
1	0	0	1	INPUT	OUTPUT	9	OUTPUT	INPUT
1	0	1	0	INPUT	OUTPUT	10	INPUT	OUTPUT
1	0	1	1	INPUT	OUTPUT	11	INPUT	INPUT
1	1	0	0	INPUT	INPUT	12	OUTPUT	OUTPUT
1	1	0	1	INPUT	INPUT	13	OUTPUT	INPUT
1	1	1	0	INPUT	INPUT	14	INPUT	OUTPUT
1	1	1	1	INPUT	INPUT	15	INPUT	INPUT

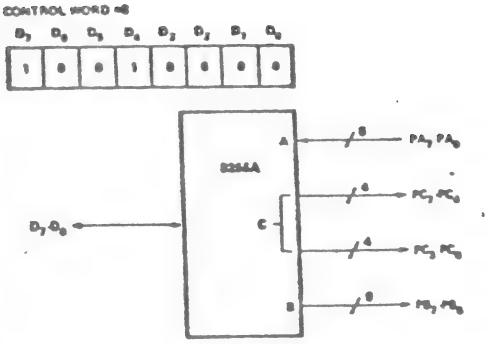
MODE 0 Configurations



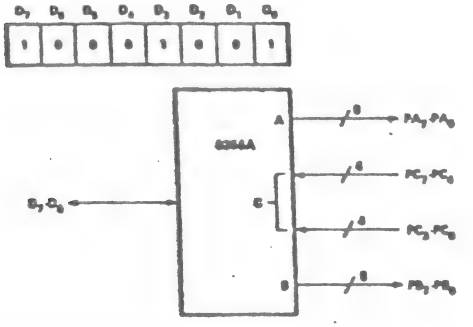
CONTROL WORD =4



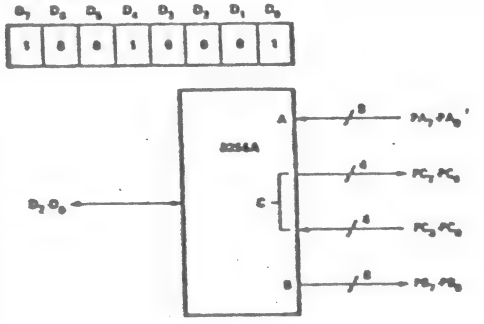
CONTROL WORD =6



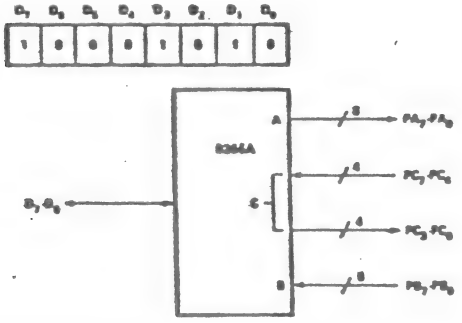
CONTROL WORD =5



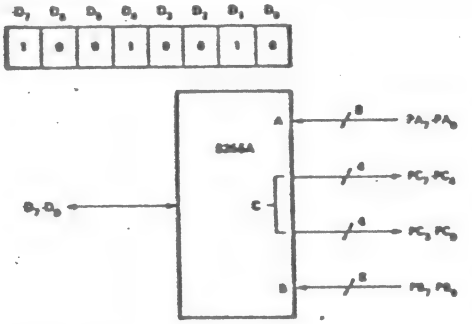
CONTROL WORD =9



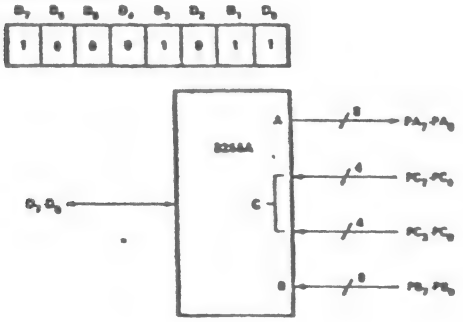
CONTROL WORD =5



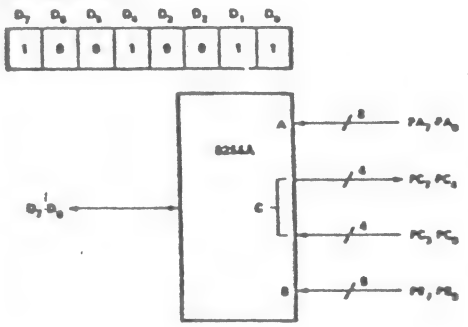
CONTROL WORD =10

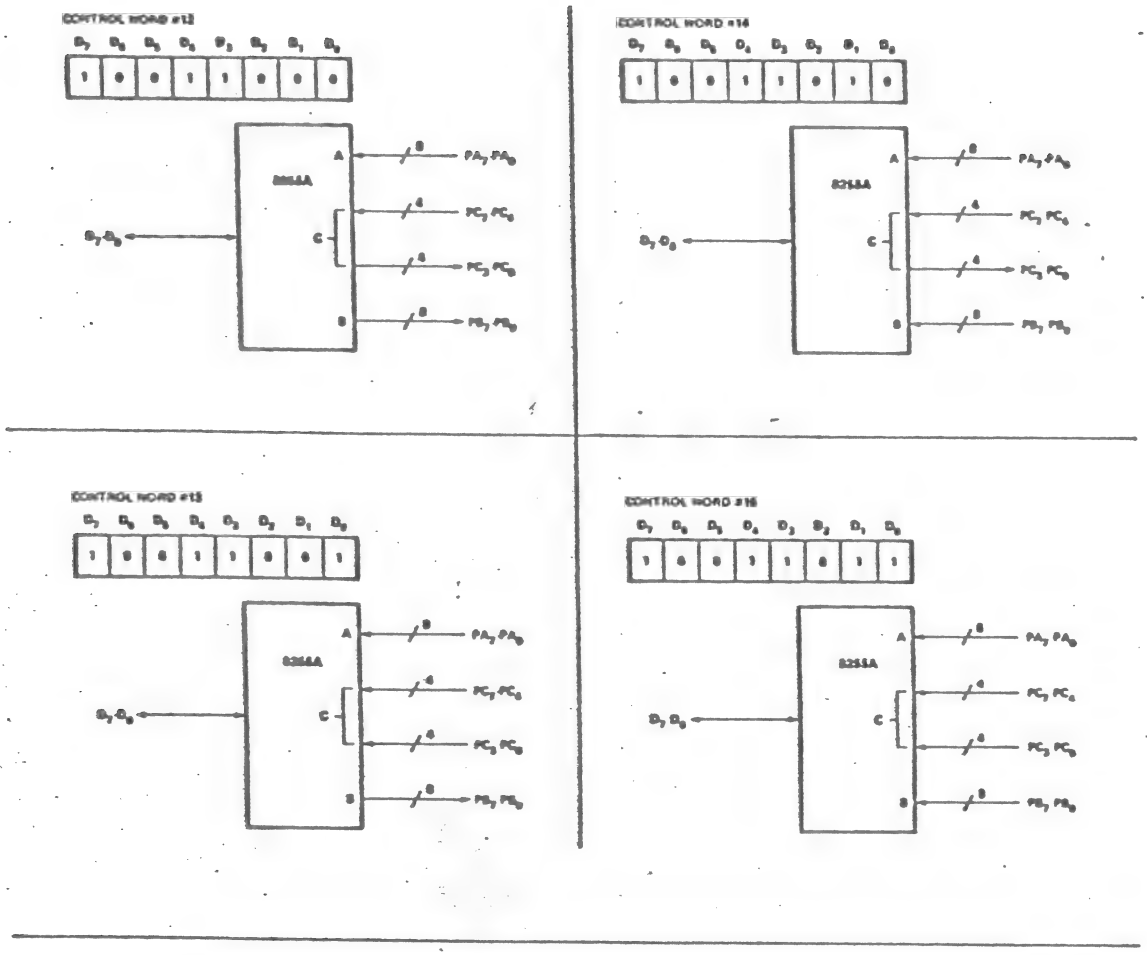


CONTROL WORD =7



CONTROL WORD =11





Operating Modes

MODE 1 (Strobed Input/Output). This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In mode 1, port A and Port B use the lines on port C to generate or accept these "handshaking" signals.

Mode 1 Basic Functional Definitions:

- Two Groups (Group A and Group B)
- Each group contains one 8-bit data port and one 4-bit control/data port.
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit data port.

Input Control Signal Definition

STB (Strobe Input). A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement. IBF is set by STB input being low and is reset by the rising edge of the RD input.

INTR (Interrupt Request)

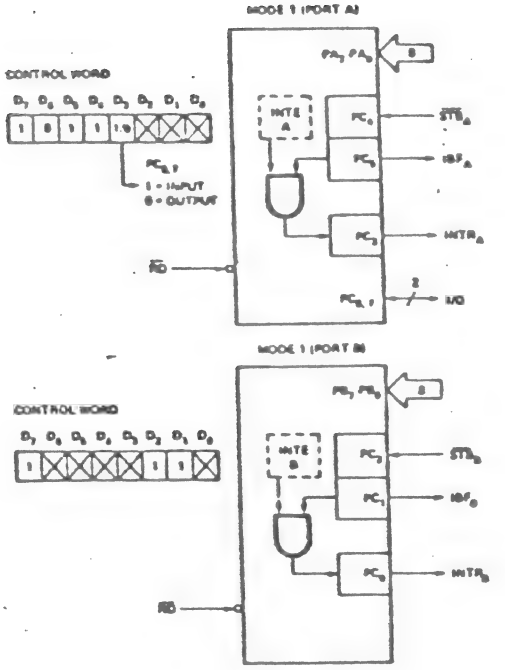
A "high" on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the $\overline{STB}$ is a "one", IBF is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{RD}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A

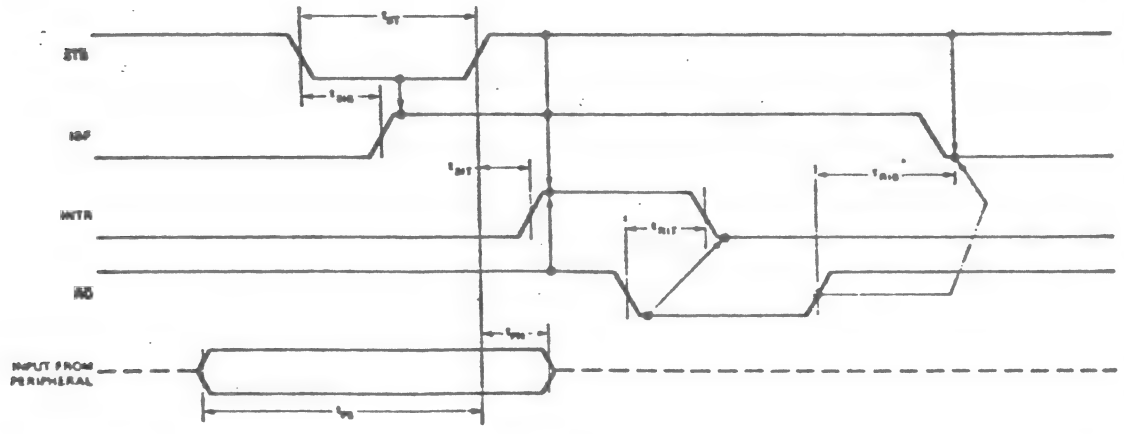
Controlled by bit set/reset of PC_4.

INTE B

Controlled by bit set/reset of PC_2.



MODE 1 Input



MODE 1 (Strobed Input)

Output Control Signal Definition

$\overline{OBF}$ (Output Buffer Full F/F). The OBF output will go "low" to indicate that the CPU has written data out to the specified port. The OBF F/F will be set by the rising edge of the WR input and reset by ACK input being low.

$\overline{ACK}$ (Acknowledge Input). A "low" on this input informs the 8255A that the data from port A or port B has been accepted. In essence, a response from the peripheral device indicating that it has received the data output by the CPU.

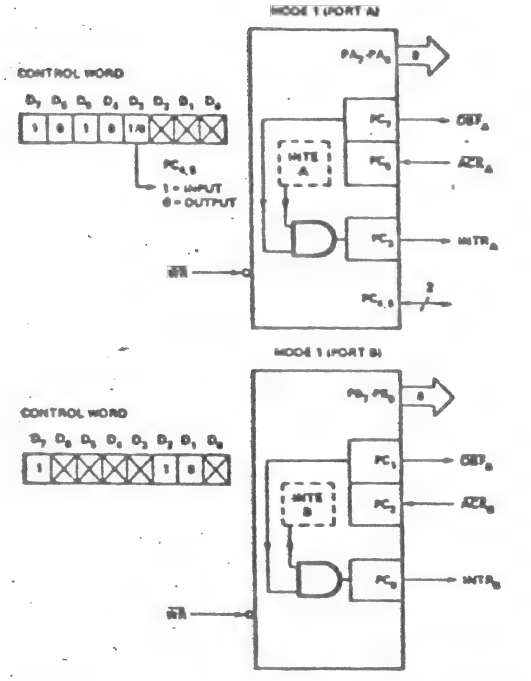
INTR (Interrupt Request). A "high" on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when ACK is a "one", OBF is a "one" and INTE is a "one". It is reset by the falling edge of WR.

INTE A

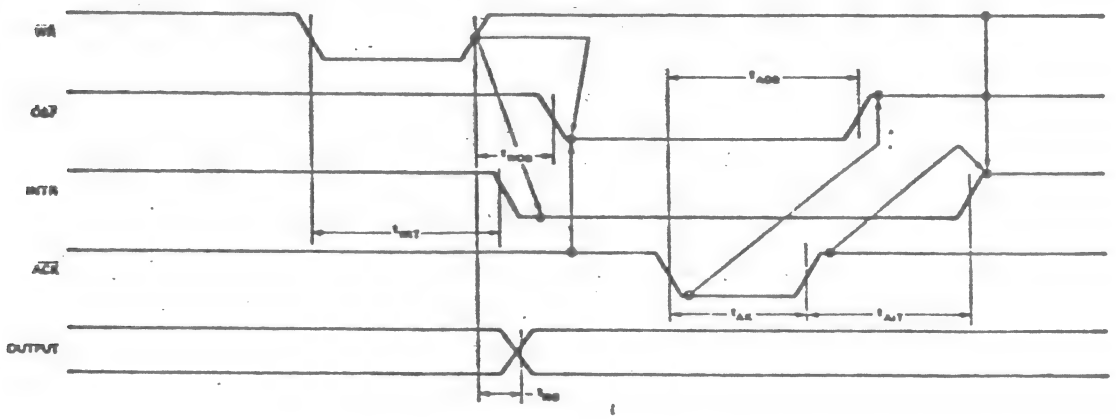
Controlled by bit set/reset of PC_6.

INTE B

Controlled by bit set/reset of PC_2.



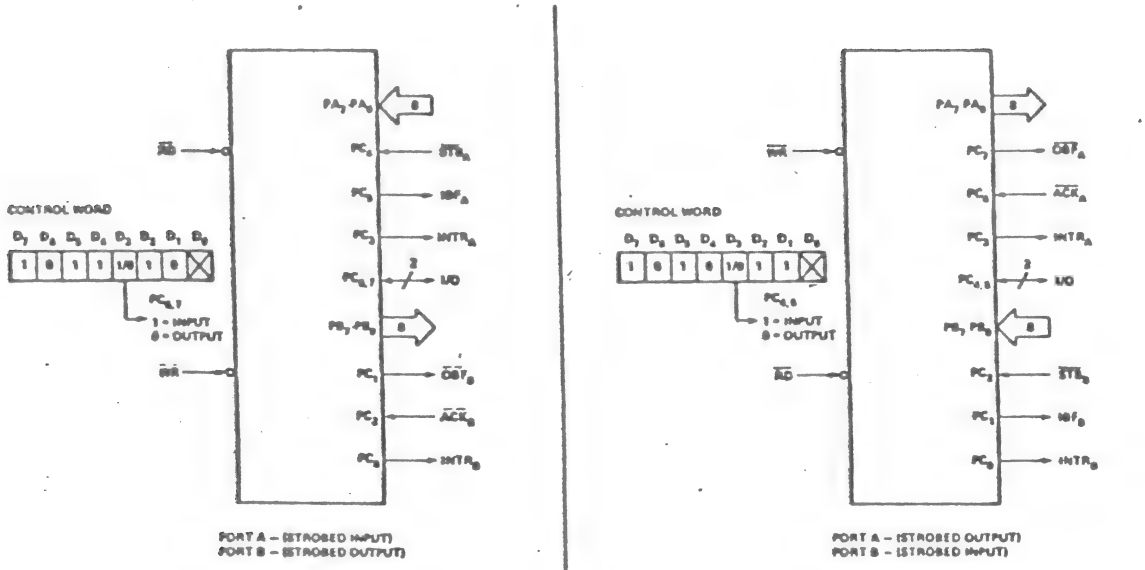
MODE 1 Output



Mode 1 (Strobed Output)

Combinations of MODE 1

Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.



Combinations of MODE 1

Operating Modes

MODE 2 (Strobed Bidirectional Bus I/O). This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline in a similar manner to MODE 1. Interrupt generation and enable/disable functions are also available.

MODE 2 Basic Functional Definitions:

- Used in Group A only.
- One 8-bit, bi-directional bus Port (Port A) and a 5-bit control Port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A).

Bidirectional Bus I/O Control Signal Definition

INTR (Interrupt Request). A high on this output can be used to interrupt the CPU for both input or output operations.

Output Operations

$\overline{OBF}$ (Output Buffer Ful). The OBF output will go "low" to indicate that the CPU has written data out to port A.

$\overline{ACK}$ (Acknowledge). A "low" on this input enables the tri-state output buffer of port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

INTE 1 (The INTE Flip-Flop Associated with OBF). Controlled by bit set/reset of PC_6.

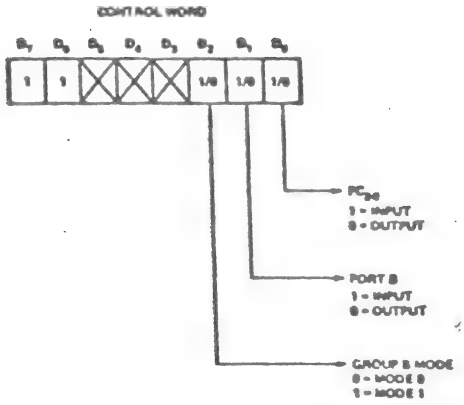
Input Operations

$\overline{STB}$ (Strobe Input)

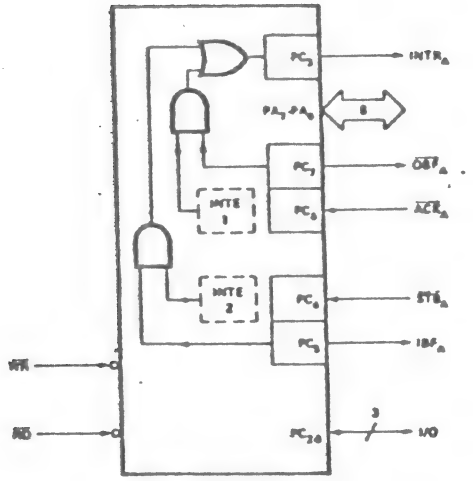
STB (Strobe Input). A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F). A "high" on this output indicates that data has been loaded into the input latch.

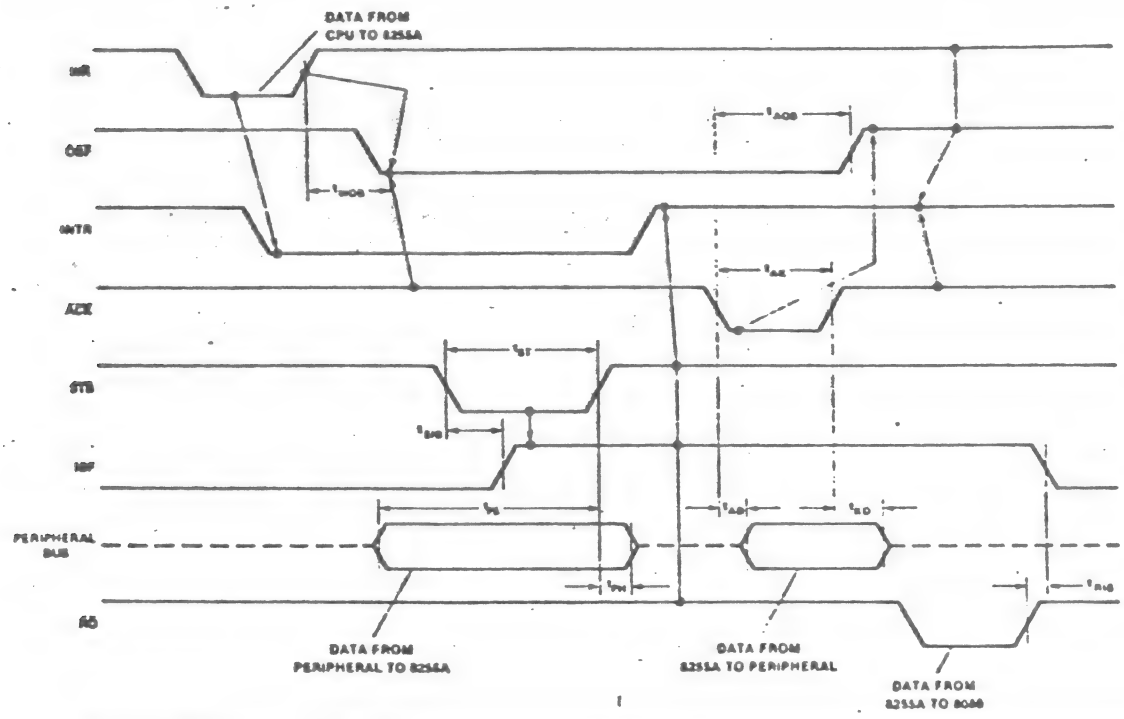
INTE 2 (The INTE Flip-Flop Associated with IBF). Controlled by bit set/reset of PC_4.



MODE Control Word



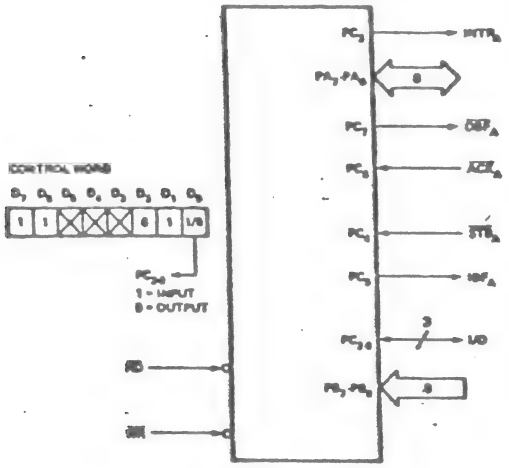
MODE 2



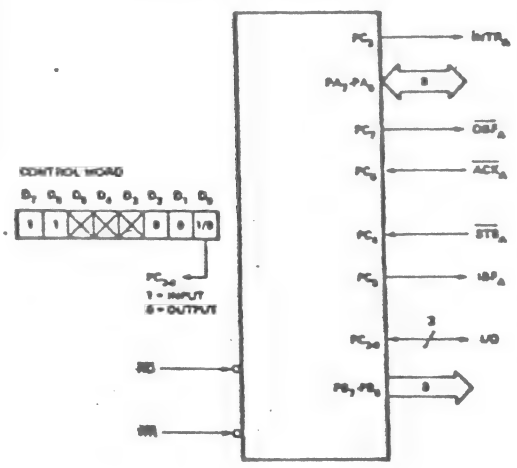
MODE 2 (Bidirectional)

NOTE: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
(INTR = IBF • $\overline{MASK}$ • $\overline{STB}$ • $\overline{RD}$ + $\overline{OBF}$ • $\overline{MASK}$ • $\overline{ACK}$ • $\overline{WR}$)

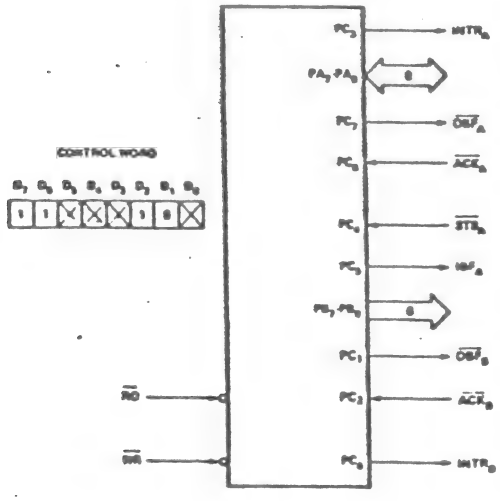
MODE 2 AND MODE 0 (INPUT)



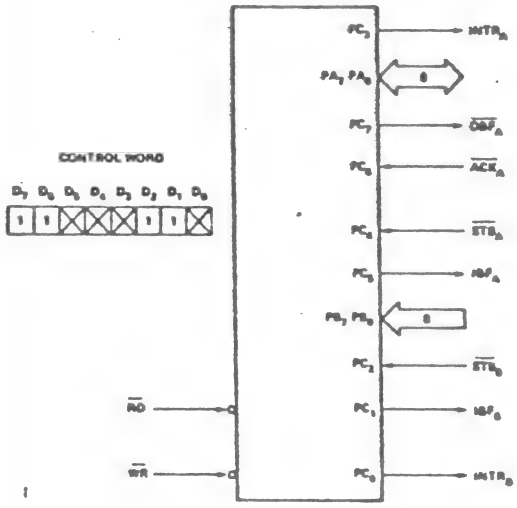
MODE 2 AND MODE 0 (OUTPUT)



MODE 2 AND MODE 1 (OUTPUT)



MODE 2 AND MODE 1 (INPUT)



MODE 2 Combinations

Mode Definition Summary

	MODE 0		MODE 1		MODE 2	
	IN	OUT	IN	OUT	GROUP A ONLY	
PA_0	IN	OUT	IN	OUT	↔	
PA_1	IN	OUT	IN	OUT	↔	
PA_2	IN	OUT	IN	OUT	↔	
PA_3	IN	OUT	IN	OUT	↔	
PA_4	IN	OUT	IN	OUT	↔	
PA_5	IN	OUT	IN	OUT	↔	
PA_6	IN	OUT	IN	OUT	↔	
PA_7	IN	OUT	IN	OUT	↔	
PB_0	IN	OUT	IN	OUT	—	MODE 0 OR MODE 1 ONLY
PB_1	IN	OUT	IN	OUT	—	
PB_2	IN	OUT	IN	OUT	—	
PB_3	IN	OUT	IN	OUT	—	
PB_4	IN	OUT	IN	OUT	—	
PB_5	IN	OUT	IN	OUT	—	
PB_6	IN	OUT	IN	OUT	—	
PB_7	IN	OUT	IN	OUT	—	
PC_0	IN	OUT	$INTR_B$	$INTR_B$	I/O	
PC_1	IN	OUT	IBF_B	$\overline{OBF}_B$	I/O	
PC_2	IN	OUT	$\overline{STB}_B$	$\overline{ACK}_B$	I/O	
PC_3	IN	OUT	$INTR_A$	$INTR_A$	$INTR_A$	
PC_4	IN	OUT	$\overline{STB}_A$	I/O	$\overline{STB}_A$	
PC_5	IN	OUT	IBF_A	I/O	IBF_A	
PC_6	IN	OUT	I/O	$\overline{ACK}_A$	$\overline{ACK}_A$	
PC_7	IN	OUT	I/O	$\overline{OBF}_A$	$\overline{OBF}_A$	

Special Mode Combination Considerations

There are several combinations of modes when not all of the bits in Port C are used for control or status. The remaining bits can be used as follows:

If Programmed as Inputs –
All input lines can be accessed during a normal Port C read.

If Programmed as Outputs –
Bits in C upper (PC_7-PC_4) must be individually accessed using the bit set/reset function.

Bits in C lower (PC_3-PC_0) can be accessed using the bit set/reset function or accessed as a threesome by writing into Port C.

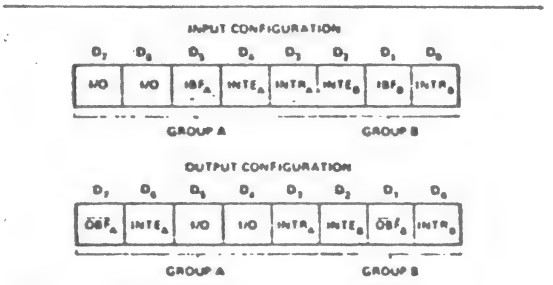
Source Current Capability on Port B and Port C

Any set of eight output buffers, selected randomly from Ports B and C can source 1mA at 1.5 volts. This feature allows the 8255 to directly drive Darlington type drivers and high-voltage displays that require such source current.

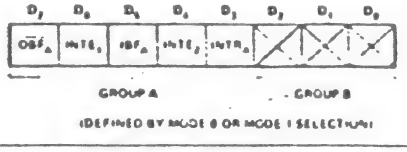
Reading Port C Status

In Mode 0, Port C transfers data to or from the peripheral device. When the 8255 is programmed to function in Modes 1 or 2, Port C generates or accepts "hand-shaking" signals with the peripheral device. Reading the contents of Port C allows the programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

There is no special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.



MODE 1 Status Word Format

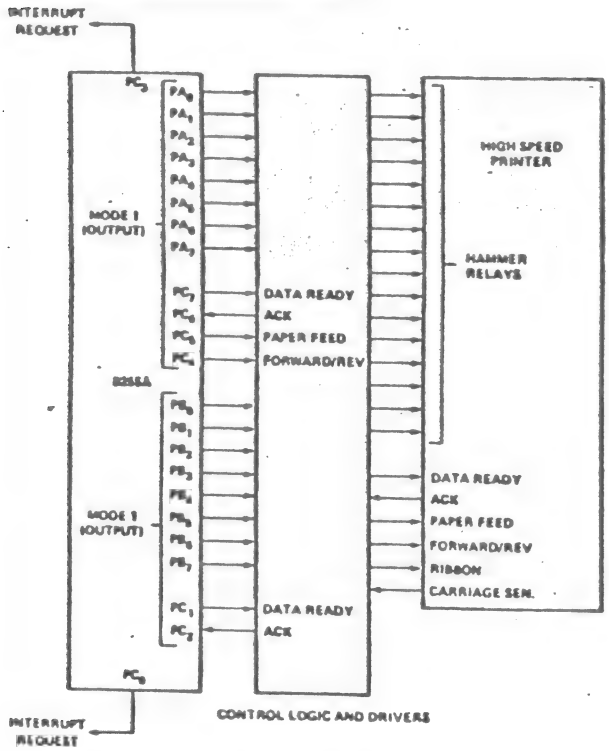


MODE 2 Status Word Format

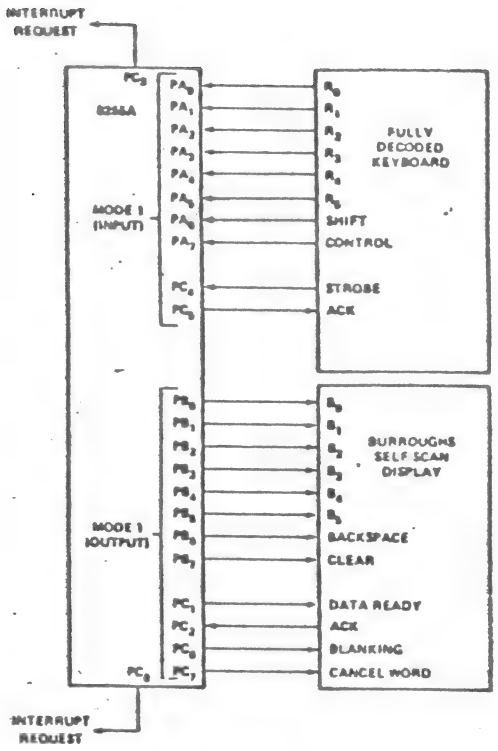
APPLICATIONS OF THE 8255A

The 8255A is a very powerful tool for interfacing peripheral equipment to the microcomputer system. It represents the optimum use of available pins and is flexible enough to interface almost any I/O device without the need for additional external logic.

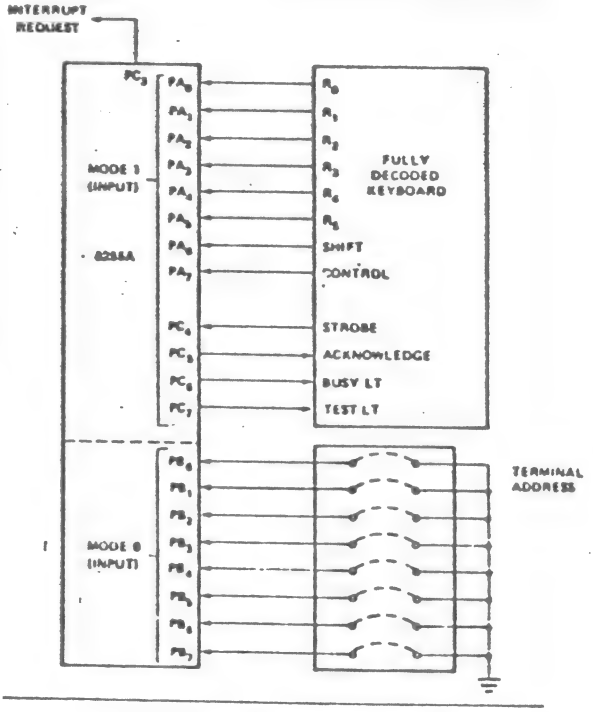
Each peripheral device in a microcomputer system usually has a "service routine" associated with it. The routine manages the software interface between the device and the CPU. The functional definition of the 8255A is programmed by the I/O service routine and becomes an extension of the system software. By examining the I/O devices interface characteristics for both data transfer and timing, and matching this information to the examples and tables in the detailed operational description, a control word can easily be developed to initialize the 8255A to exactly "fit" the application. Figures 17 through 23 present a few examples of typical applications of the 8255A.



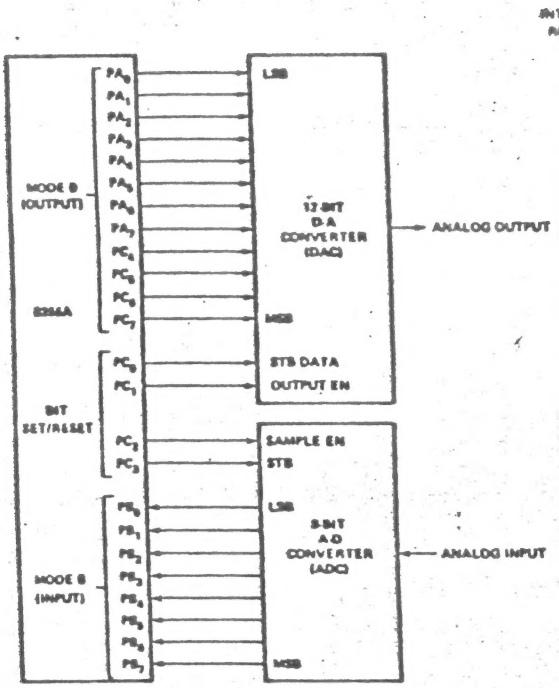
Printer Interface



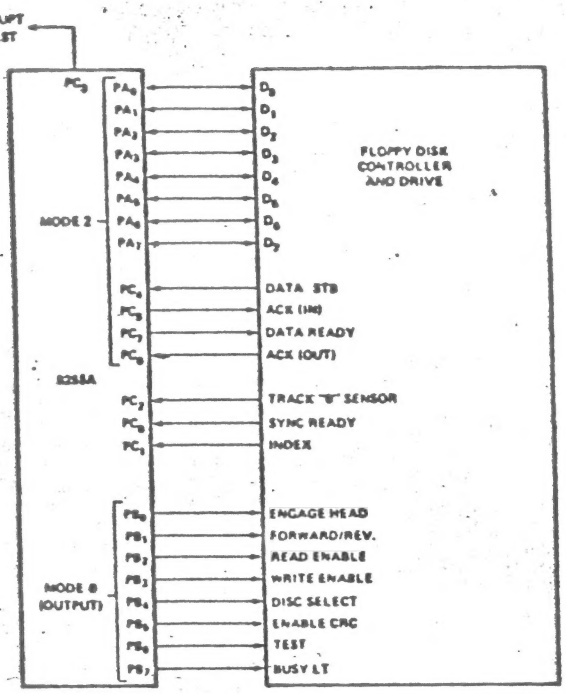
Keyboard and Display Interface



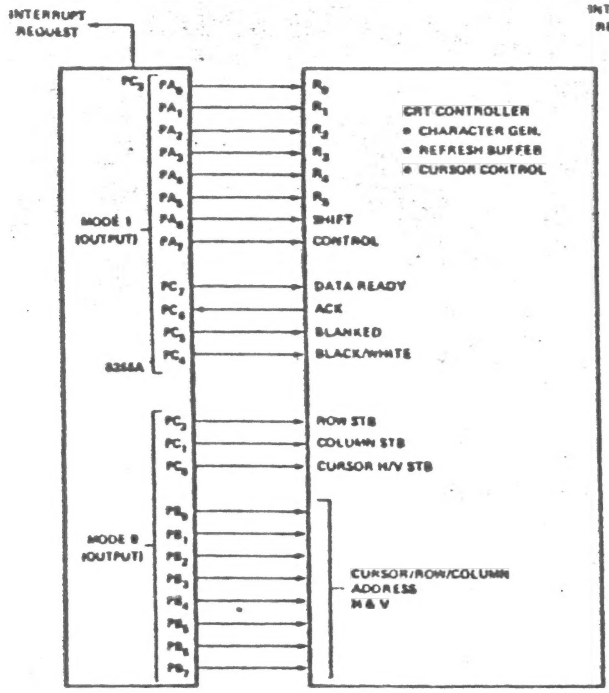
Keyboard and Terminal Address Interface



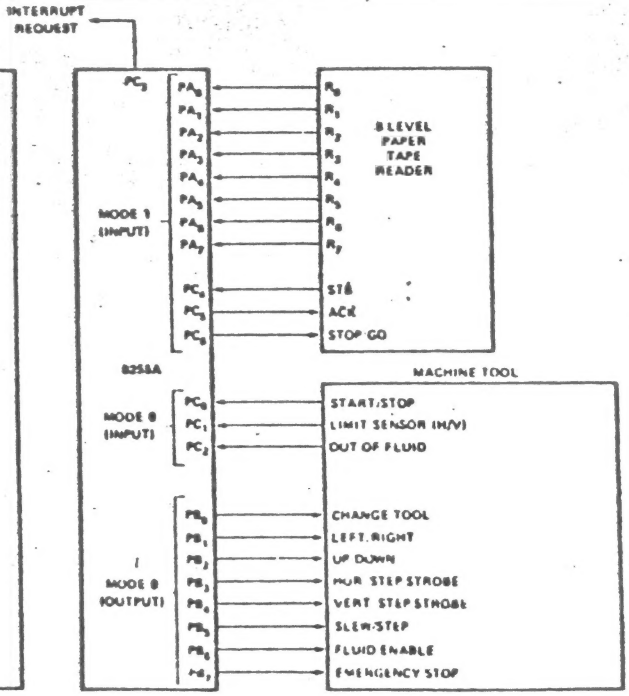
Digital to Analog, Analog to Digital



Basic Floppy Disc Interface



Basic CRT Controller Interface



Machine Tool Controller Interface

WH89-PAL

PARTS LIST

IC'S

1 X 443-728	74LS00
1 X 443-885	74LS245
1 X 443-8255	8255A PARALLEL I/O

CONNECTORS

1 X 432-947	25 pin female buss connector
1 X 432-1023	10 pin female buss connector
3 X 432-984	10 pin male cable connector

IC SOCKETS

1 X 434-253	40 pin IC socket
1 X 434-310	20 pin IC socket
1 X 434-298	10 pin IC socket

CAPACITORS

1 X 21-47	.01uf 50v cer. capacitor
1 X 25-220	10uf 20v tan. capacitor

MISC.

1 X 885-PAL	Double sided ckt. board
1 X 421-.2A	.2A fuse
1 X 434-.2A	Ckt. board fuse holder

All of the above parts can be ordered from.....

Heath Germany
Robert Bosch Str. 32-38
D-6072 DREIEICH, W. GERMANY

CABLE CONFIGURATION IDEAS

Because a parallel I/O interface is used for so many different applications and configurations and because there is no 'standard' pin configuration for a parallel I/O cable, a cable has not been included with the WH89-PAL. However here is a basic layout that you may wish to incorporate into your system.

All parts are listed and are available from you local Heath operation or from the two addresses listed at the end of this manual.

PIN	PORT 'A'	PORT 'B'	PORT 'C'
	1 = A0	09 = B0	17 = C0
	2 = A1	10 = B1	18 = C1
	3 = A2	11 = B2	19 = C2
	4 = A3	12 = B3	20 = C3
	5 = A4	13 = B4	21 = C4
	6 = A5	14 = B5	22 = C5
	7 = A6	15 = B6	23 = C6
	8 = A7	16 = B7	24 = C7

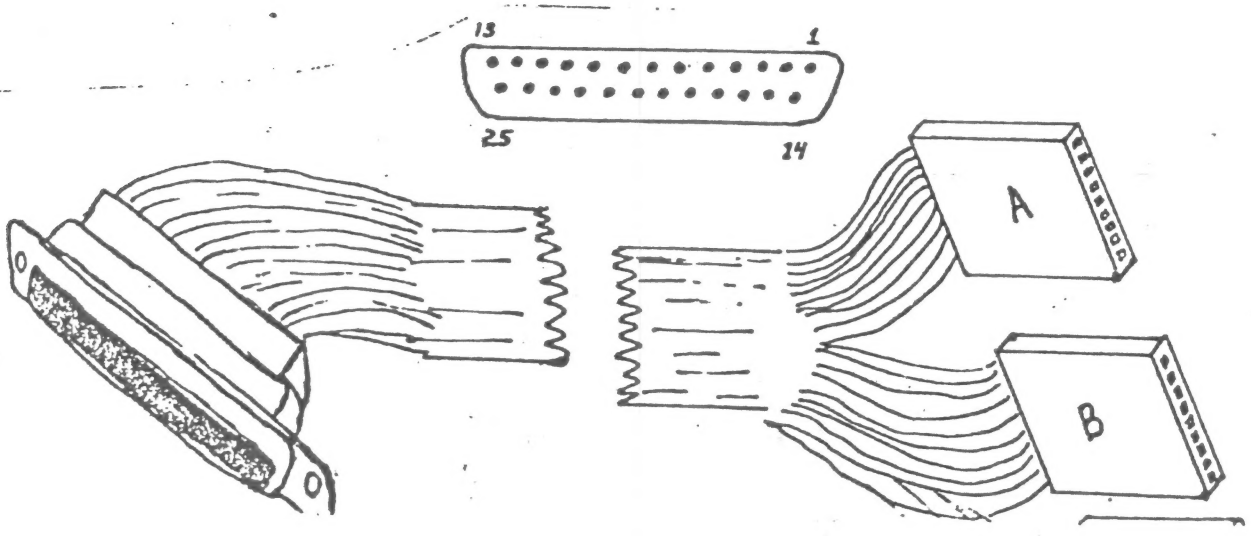
25 = GROUND

PARTS

1 X 432-1032	Male 'D' connector
30 X 432-1033	Male 'D' connector pins
3 X 432-958	Female Molex (r) shells
30 X 432-866	Female Molex (r) pins

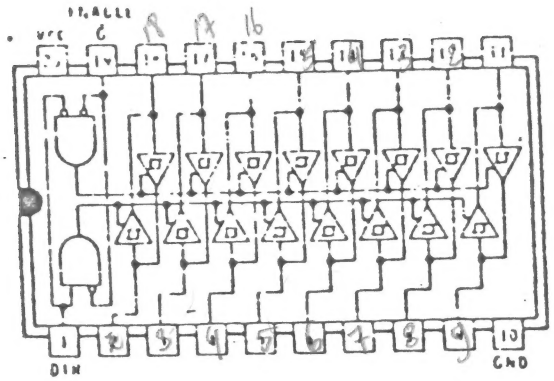
.5 meters of 25 wire ribbon cable, or 25 wire round cable.

('D' connector seen from back.)

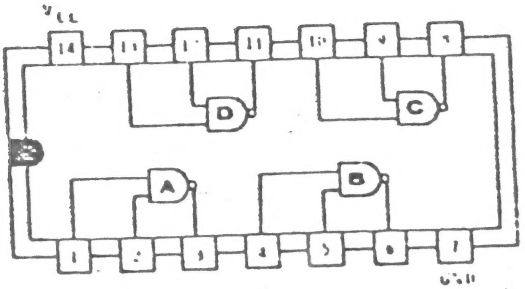


IC Pinouts

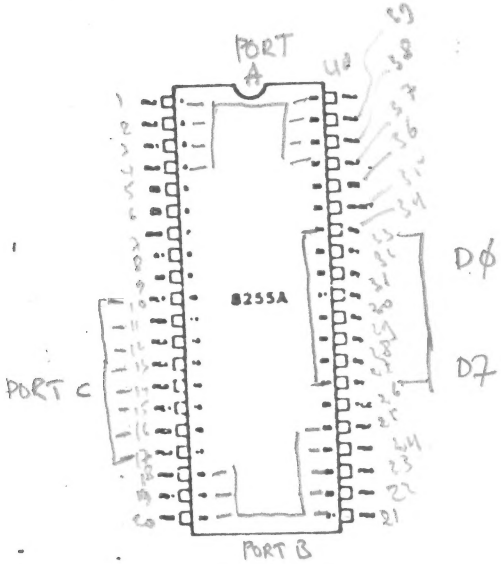
IC2 443-885 74LS245



IC3 443-728 74LS00



IC1 443-8255 8255A



PIN NAMES

D_0-D_7	DATA BUS (BI-DIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA0-PA7	PORT A (BIT)
PB0-PB7	PORT B (BIT)
PC0-PC7	PORT C (BIT)